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DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4027B flip-flops Dual JK flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Philips



PHILIPS

FAIRCHILD
SEMICONDUCTOR

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

August 2012

LM78XX/LM78XXA — 3-Terminal 1A Positive Voltage Regulator

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220 (Single Gullwing)	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT			
LM7806ACT	±2%		0°C to +125°C
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

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LM78XX/LM78XXA Rev. 1.2



BC557, 557B

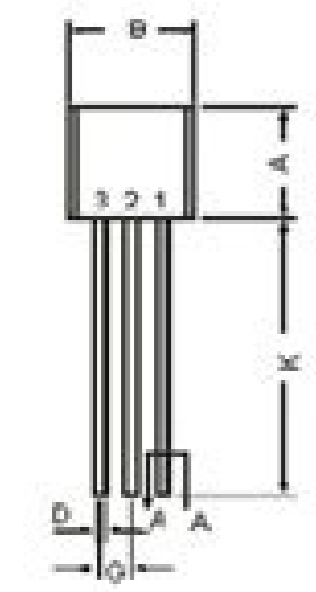
General Purpose Transistor



Features:

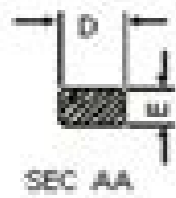
- PNP Silicon Planar Epitaxial Transistors.
- Especially Suited For use in Driver Stages of Audio Amplifiers, Low Noise Input Stages of Tape Recorders, Hi-Fi Amplifiers, Signal Processing Circuits of Television Receivers.

TO-92 Plastic Package



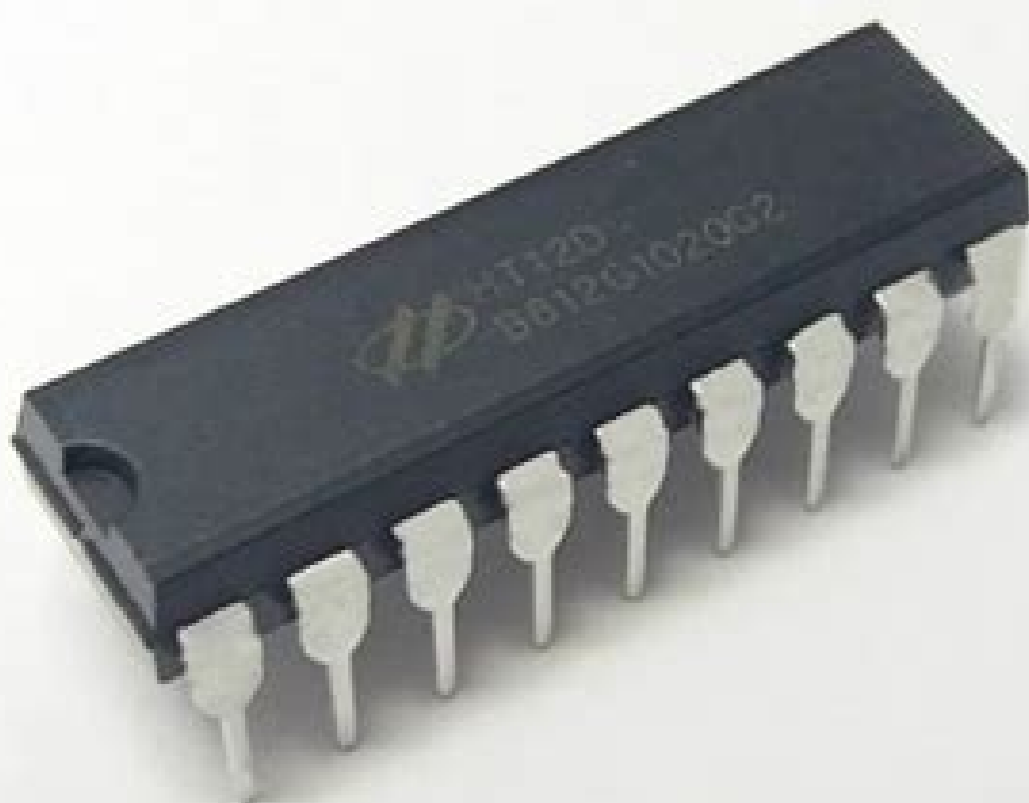
Dimensions	Minimum	Maximum
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5*	
G	1.14	1.40
H	1.53	
K	12.70	

Dimensions - Millimetres



Pin Configuration

1. Emitter
2. Base
3. Collector



Ht12d ic datasheet. Ht12d ic. Ht12d datasheet. Ht12d datasheet pdf.

Rd., Rd., Taipei, Taiwan, R.O.C. Tel: 886-2-2782-9635 Fax: 886-2-2782-9636 Fax: 886-2-2782-7128 (International sales hotline) Holtek Semiconductor (Hong Kong) Ltd. 5 0 3 . Pin Description Pin Name I/O Internal Connection Description A0~A11 I NMOS TRANSMISSION GATE Input pins for address A0~A11 setting They can be externally set to VDD or VSS. They are paired with Holtek's 212 series of encoders (refer to the encoder/decoder cross reference table). For proper operation, a pair of encoder/decoder with the same number of addresses and data format should be chosen. 48531 Warm Springs Boulevard, Suite 413, Fremont, CA 94539 Tel: 510-252-9880 Fax: 510-252-9885 Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and HT12F is used to decode 12 bits of address information. 5 0 2 . 0 0 1 . Yes C o d e i n ? For the most up-to-date information, please visit our web site at . Otherwise it is always low. The decoders will then check the received address three times continuously. Holtek Semiconductor Inc. The content and copyrights of the attached material are the property of its owner. They compare the serial input data three times continuously with their local addresses. 0 0 3 . A correct device should be chosen according to the requirements of the individual addresses and data. 5 0 4 . The applications mentioned herein are used solely for the purpose of illustration and Holtek makes no warranty or representation that such applications will be suitable without further modification, nor recommends the use of its products for application that may present a risk to human life due to malfunction or otherwise. Part No. Data Pins Address Pins Output Type Operating Voltage HT12D 4 8 Latch 2.4V~12V HT12F 0 12 3/4 2.4V~12V Flowchart The oscillator is disabled in the standby state and activated when a logic high signal applies to the DIN pin. 212 Series of Decoders 9 July 1999 Copyright © 1999 by Holtek Semiconductor Inc. 5 0 (1 0 K H Z) 1 . 0 0 2 . The 212 series of decoders are able to decode information consisting of N bits of addresses and 12 n bits of data. Max. 1 D Valid transmission. 7th floor, building 2, No.889, Yi Shan Road, Shanghai, China Tel: 021-6485-5560 Fax: 021-6485-0313 Holmate Technology Corp. 2 5 2 3 4 5 6 7 8 9 1 1 1 1 1 1 2 1 3 V D (V D C) 6 8 K 6 2 K 5 6 K 5 1 K 4 7 K 3 9 K 3 6 K 3 3 K 3 3 0 K 2 7 K 7 7 K 7 5 K 8 2 K 1 0 K 1 2 0 K 1 5 0 K 1 8 0 K 2 0 K 9 The HT12D, on the other hand, provides 4 pins of data of type of pestle whose data remain unchanged until new data is received. 1. The functional functioning of this development in other conditions beyond those listed in the specification is not implied prolonged prolonged Tupni C&E"à,521 of c&E "à05.....erutarepmet egarots v31 of v30.....egatlov ylipus sgnitar mumixam elasha stuchic noitennoc lanretni etamixorppa yippus rewpov evittsop à3, 2CSO nip tupni rotallico ROTALLICSO I ICSD high evitca ,noissimsnart dilav TUO SOMC O TV nip tupni atad laireS NI SOMC I NID snip atad tuptuo TUO SOMC O 11D~8D. niM snoitidnoC tseT retemarP lobmyS C&E"à52~at scilsiretcarahC lacirtoeE. delibresed snoitacifceps eht fo esu eht moof gnistra yillibisnosper on semussa keltoH ,revevoh 7 r o r r e a t a d r o s s e r d d a s e Y o N s e Y d r o w s h I f o t s e r e h t e r o n g i s T v e l b a s i d e d o m y d n a t s e Y o N o N s e Y o N a t a d e r o t S 3 847321 rebmuN traP ocemaj Smesys LORTNOC ETOMER REHTO à-à Senohpolet Seldroc à-à, Metsys Yiruces à-à àla Rac à-à, S, S, Shirellitnoc rood alag srellitnoc srellitnoc shrellitnoc rodnoc rodnoc sellorltnoc rodnoc rodnoc sellorltnoc rodnoc sellorltnoc rodnoc selstrolotnoc rodnoc roct to Metsys Mrala Erif Dna Erif DNA à-à, Metsys Mrala Ralrub à-à, Snoitacilppa senops snenrexe lamim à-à, Mustiam Rotallisco ni-Tliub à-à, Yno stidda 21 :F21th - STIB ATAD 4 DNA DNA stibs 8 :d21th - Noitibnoc rebrum you are , Sredocne Fo Seires 21 2 s&E"à&E"à&E"à&E"à&E htiw à-à 21 ndiocec FO Elhapac à-à 2 sson hson somc .2 .egatlov gniatlov gniatlov à-à, Serutaf .TUPNI OLAND ON EREHT FIL WOL TEB EB DLUOHS nid ,yes ot taht .deviecer of Oil on Rotoc sselda ROF SISL SOMC FO SEIRES A ERA SRECED 21 2 eht noitpircs lareneg , I'm not gonna let you go I transferred to the output pins. Holtek reserves the right to alter its products without prior notification. 212 Series of Decoders 3 July 12, 1999 N M O S T R A N S M I S I O N G A T E C M O S I N O S C I L L A T O R O S C I O S C 2 C M O S O U T E N 5 . A signal on the DIN pin activates the oscillator which in turn decodes the incoming address and data. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. 0 0 0 . Distributed by: www.jameco.com &A"à 1-800-831-4242 2. The decoders receive serial addresses and data from a programmed 212 series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. 212 Series of Decoders 5 July 12, 1999 Functional Description Operation The 212 series of decoders provides various combinations of addresses and data pins in different packages so as to pair with the 212 series of encoders. VT can be used as a momentary data output. Output type Of the 212 series of decoders, the HT12F has no data output pin but its VT pin can be used as a momentary data output. Oscillator frequency vs supply voltage The recommended oscillator frequency is 10KSCD (decoder) @ 50 KOSCE (HT12E encoder) @ 13 KOSCE (HT12A encoder). (Headquarters) No.3 Creation Rd. II, Science-based Industrial Park, Hsinchu, Taiwan, R.O.C. Tel: 886-3-563-1999 Fax: 886-3-563-1189 Holtek Semiconductor Inc. L a t c h d a t a t o o u t p u t & a c t i v a t e V T A d d r e s s b i t s m a t c h e d ? The information appearing in this Data Sheet is believed to be accurate at the time of publication. The output of the VT pin is high only when the transmission is valid. Decoder timing Encoder/Decoder cross reference table Decoders Part No. Data Pins Address Pins VT Pair Encoder Package Encoder Decoder DIP SOP DIP SOP HT12D 4 8 A A HT12A 18 20 18 20 HT12E 18 20 HT12F 0 12 A A HT12A 18 20 18 20 HT12E 18 20 Address/Data sequence The table provides direction/data sequence for various models of the 212 series of decoders. Decoders receive data transmitted by a coder and interpret the first nbits of the code period as addresses and the last 12 nbits as data, where n is the address code number. If all the address codes received match the content of the local address of the decoder, the 12 N bits of data are decoded to activate the output pins and the VT pin is set high to indicate a valid transmission. RM.711, Tower 2, Cheung Sha Wan Plaza, 833 Cheung Sha Wan Rd., Kowloon, Hong Kong Tel: 852-2-745-8288 Fax: 852-2-742-8657 Holtek Semiconductor (Shanghai) Ltd. (c) (c) A3 A4 A5 A6 D8 D10 D11 HT12F A0 A1 A3 A6 d d d / l M a t c h r e v i o s t e r e d a t a ? Appropriation of pin 212 Decoder series 2 July 1999 d a t a s h i f t r e g i s t e r o s c l a t o r b u f e r s y n c . .

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